

ABSTRACT OF THE DISCLOSURE

An address buffer only having $(N/2)$ stages, capable of performing the same function as that of an N -stage address buffer is provided. The address buffer used in a semiconductor device having N (where N is a natural number) additive latency comprises $(N/2)$ serially-
5 connected flip-flops, and an address control circuit which generates an address enable signal in response to a clock signal and a command signal. Each of the $(N/2)$ flip-flops is clocked to the address enable signal and sequentially latches an external address.